



Chipset for Remote Digital Capture of Noisy Signals

For Improved Data Transmission over Fiber and Wireless

Seeking Technology Development Partnership

The NRAO has perfected a method for the transmission of raw sampled data over fiber without any of the pre-formatting or encoding normally required, greatly reducing the overhead at the detector. Instead, the link is managed at the receive end of the fiber using the well-known statistics of random noise which is always present in the applicable data streams. All that is needed at the source is an Analog-to-Digital Converter (ADC), a no-frills serializer, and a laser diode with associated driver or modulator. No microprocessor or other complex logic is required.

Using a patented algorithm (US# 8,688,617) developed at NRAO, two separate custom integrated circuits (ICs) will be designed. The first is an ADC with "true-serial" output, where unformatted samples are delivered continuously in real-time on a single output channel at fiber-link data rates – 2.5 Gbps minimum with a goal of 10 Gbps.

The second custom IC will be a de-serializer operating at 2.5 Gbps or 10 Gbps, depending on that achieved by the ADC. It will incorporate specialized sample-boundary detection circuitry to deliver properly aligned samples at the output with no prior formatting or user intervention.

Prototype Integrated Receiver using the new unformatted fiber optic link



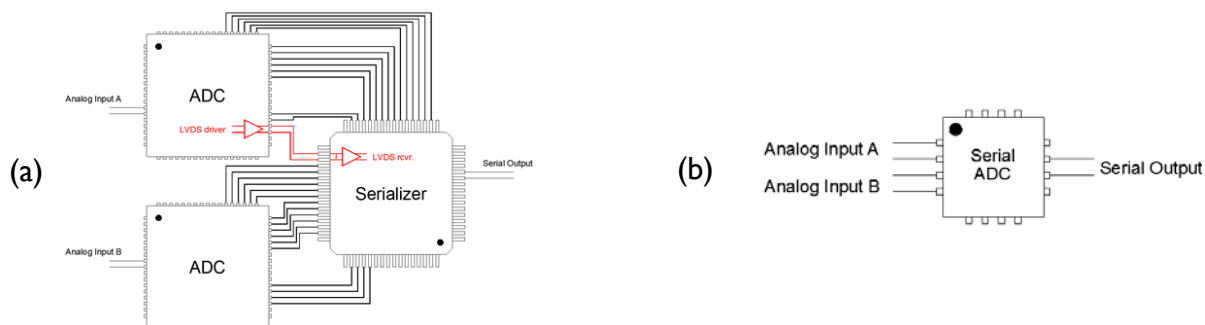
Potential Implementations

- An ultra-miniature imaging sensor with high data-rate wireless digital connection to a host device or processor (over an unlicensed band). Somewhat like a Bluetooth device except with 100-1000 times the data rate.
- A chipset for an "ADC-on-a-fiber" consisting of the Serial-ADC at one end, possibly with an integrated laser driver, and the deserializer with built-in word-boundary detection and automatic alignment at the other.
- As a protocol embedded in FPGA interfaces, particularly those designed for computational signal processing. Perhaps this takes the form of an "IP block" that can be used in such FPGAs.
- A handheld or otherwise compact imaging scanner (medical, scientific, or security).
- As a method embedded within an integrated radiometer (as in the radio astronomy application for which it was developed) using off-the-shelf components.

Major Benefits

By combining the ADC and Serializer, the layout of the application circuit becomes independent of the bit-resolution of the sampler. It should also be possible using the NRAO algorithm to determine not only where the sample boundaries exist, but how frequent they are, in effect determining the bit-resolution dynamically. The NRAO solution opens the door for resolution-agnostic architectures wherein the bit-resolution can be traded against sample rate on-the-fly in order to respond to transient events or changing environmental conditions.

Illustration of power and space-savings realized in the sensor module by integrating the ADC and serializer functions onto a single chip. (a) Current 2-channel solution using off-the-shelf parts. (b) Proposed single-chip solution.





Why it Matters

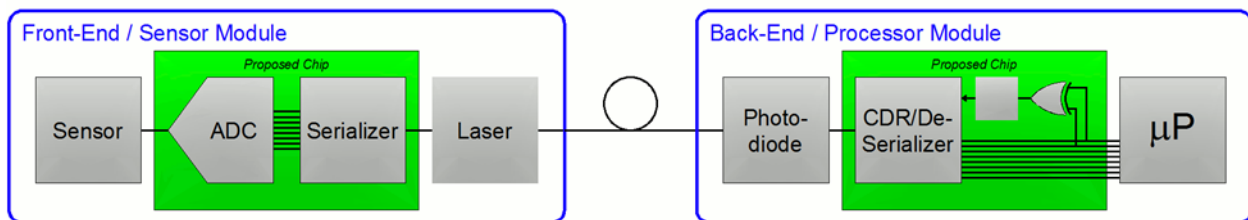
With the advent of modern computing, it is common practice in almost all scientific, medical, aerospace, industrial, and military applications where sensors collect data from the environment for that information to be digitized and processed by numerical algorithms. In many cases, the processor itself is either too large and immobile, too power hungry, or emits too much interference to be integrated directly with the sensors.

Optical fiber is often the preferred medium for transmission if the bandwidth is large, even over a distance of a few tens of meters, and digital transmission is favored over analog for maximum fidelity. Conventional digital links, however, incur a substantial overhead at the source and may be prohibitive for high aggregate data rates. Because of the substantial overhead, a niche market for analog-only fiber optic links, even where digital links would otherwise be preferable, has emerged.

Technical Description

Conventional digital data links are designed to transmit *arbitrary* data, where nothing is assumed about the content. Therefore, formatting is applied to give the bit stream certain desirable characteristics, such as DC balance and sufficiently high transition density to ensure reliable clock recovery. Analysis has shown, however, that data streams acquired by directly sampling noisy signals already possess these properties. It is therefore possible to pass the bit stream across a serial link with nothing more than a serializer connected to the ADC. No intervening logic is necessary.

In the process of recovering the clock at the other end, however, some unknown number of the initial bits have been lost. While a brief loss of data during startup is unimportant, the loss of the logical boundaries between samples is critical. Conventional data links overcome these issues by packetizing or framing – by inserting recognizable codes in the data stream to mark the beginning and the end of chunks of data. Lacking such encoding in our scheme, we rely instead on the statistical properties of Gaussian noise (prevalent in at least the background of almost all sensor data) to identify the most-significant bits (MSB).



Schematic of a typical application highlighting the proposed chipset: an ADC/Serializer in the front-end, and a Deserializer with MSB-detection in the back-end.

Current Status of Development

A bench-top proof-of-concept has already been built and tested using off-the-shelf components. Further improvement in size, power dissipation, and RFI environment near the sensor could be realized with a custom chipset optimized for this purpose. Specifically, what is needed is an ADC with high-speed serial output for use at the transmit end, and a custom clock-recovery/de-serializer at the receive end to parse the data stream according to the patented algorithm developed at NRAO. This would effectively give system designers an "ADC on a fiber" to incorporate in their own applications without having to know the details of its implementation.

Benefits

- Simple implementation at receive-end requires only a handful of logic gates and a leaky integrator in addition to standard clock-recovery circuit
- Offers the fidelity of a digital link with greatly reduced bulk, complexity, and power consumption
- Reduced power consumption by eliminating parallel LVDS chip-to-chip interface

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